AMENDMENTS TO CLAIMS

1. (Withdrawn) A clustered computer system comprising:

a plurality of central processing units (CPU) and memory installed apparatuses having at least one CPU and at least one memory;

a plurality of input/output control apparatuses; and

a plurality of diagnostic control circuits, each diagnostic control circuit of said plurality of diagnostic control circuits being connected with one of said plurality of the CPU and memory installed apparatuses, and with one of said plurality of input/output control apparatuses, and each of said plurality of diagnostic control circuits being connected to one another,

wherein said CPU and memory installed apparatuses and said input/output control apparatuses are connected to each other by a network,

wherein said CPU and memory installed apparatuses transmit an input/output instruction to at least one of said plurality of input/output control apparatuses assigned in advance, and

wherein when one of said plurality of diagnostic control circuits detects a fault in a connected CPU and memory installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between a non-faulty CPU and memory installed apparatus and an input/output control apparatus originally connected to a faulty CPU and memory installed apparatus.

2. (Previously presented)A computer system comprising:

a plurality of central processing units (CPU) and memory installed apparatuses having at least one CPU and at least one memory;

a plurality of input/output control apparatuses;

a plurality of diagnostic control circuits, each diagnostic control circuit of said plurality of diagnostic control circuits being connected with one of said plurality of the CPU and memory installed apparatuses, and with one of said plurality of input/output control apparatuses, and each of said plurality of diagnostic control circuits being connected to one another; and

a network connecting said CPU and memory installed apparatuses and said input/output control apparatuses to each other,

wherein each of said CPU and memory installed apparatuses comprises communication means for transmitting an input/output instruction issued by at least one CPU of said plurality of CPU and memory installed apparatuses to at least one of said input/output control apparatuses assigned in advance to said at least one CPU and memory installed apparatuses via said network, and receives a response from at least one of said input/output control apparatuses via said network,

wherein each of said input/output control apparatuses comprises communication means for receiving an input/output instruction from at least one CPU and memory installed apparatuses assigned in advance to at least one of said plurality of input/output control apparatuses via said network, and transmits a response to said input/output instruction to said at least one CPU and memory installed apparatuses via said network, and

wherein when one of said plurality of diagnostic control circuits detects a fault in a connected CPU and memory installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between a non-faulty CPU and memory installed apparatus and an input/output control apparatus originally connected to a faulty CPU and memory installed apparatus.

3. (Previously Presented) A computer system according to claim 2, wherein said communication means of each of said input/output control apparatuses comprises:

means for receiving the input/output instruction as being effective only when the source of the input/output instruction received via said network is a CPU and memory installed apparatuses which has been set in advance.

4. (Previously Presented) A computer system according to claim 2, wherein said communication means of each of said CPU and memory installed apparatuses comprises:

means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatuses which has been set in advance.

5. (Original) A computer system according to claim 2, wherein said network is also used for communications between said plurality of CPU and memory installed apparatus.

6. (Previously Presented) A computer system according to claim 3, wherein said communication means of each of said CPU and memory installed apparatuses comprises:

means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatuses which has been set in advance.

7. (Previously Presented) A computer system according to claim 5, wherein said communication means of each of said CPU and memory installed apparatuses comprises:

means for communicating with other CPU and memory installed apparatuses via said network.

8. (Previously Presented) A computer system according to claim 7, wherein the communications between said plurality of CPU and memory installed apparatuses are communications for accessing memories installed on other CPU and memory installed apparatus.

9. (Currently amended) A computer system according to claim 2, further comprising:

means for~~, when either one of said CPU and memory installed apparatuses fails to operate due to a fault,~~ assigning said input/output control apparatuses which have ~~has~~ been used by ~~a~~ faulty CPU and memory installed apparatuses to another normal CPU and memory installed apparatuses when said faulty CPU and memory installed apparatuses fail to operate, thereby ~~hereby~~ to continue system operation.

10. (Previously Presented) A computer system according to claim 9, wherein an active one of the CPU and memory installed apparatuses which is using another input/output control apparatuses is used as said other normal CPU and memory installed apparatus.

11. (Previously Presented) A computer system according to claim 9, further comprising:

a backup CPU and memory installed apparatus, said backup CPU and memory installed apparatuses being used as said other normal CPU and memory installed apparatus.

12. (Currently amended) A computer system according to claim 2, further comprising:

at least one backup input/output control apparatus; [[,]] and

means for~~, when either active one of said input/output control apparatuses fails to operate due to a fault,~~ assigning said backup input/output control apparatuses to said CPU and memory installed apparatuses which have ~~has~~ been using ~~the~~ faulty input/output control apparatuses when said faulty input/output control apparatuses fail to operate, thereby to continue system operation.

13. (Withdrawn) A computer system comprising:

a central processing unit (CPU) and memory installed apparatuses comprising at least one CPU and at least one memory;

an input/output control apparatus;

a communication cable connecting said CPU and memory installed apparatuses and said input/output control apparatuses to each other; and

a diagnostic control circuit connected with said CPU and memory installed apparatus and with said input/output control apparatus,

wherein said CPU and memory installed apparatuses comprises communication means for transmitting an input/output instruction issued by said CPU to said input/output control apparatuses via said communication cable, and receives a response from said input/output control apparatuses via said communication cable,

wherein said input/output control apparatuses comprising communication means for receiving an input/output instruction from said CPU and memory installed apparatuses via said communication cable, and transmits a response to said input/output instruction to said CPU and memory installed apparatuses via said communication cable, and

wherein when said diagnostic control circuit detects a fault in said connected CPU and memory installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between a second non-faulty CPU and memory installed apparatus and an input/output control apparatus originally connected to a faulty CPU

and memory installed apparatus.

14. (Previously presented) A CPU and memory installed apparatuses comprising:

at least one central processing unit (CPU) and at least one memory;

communication means for communicating with an external circuit comprising an input/output control apparatus, transmitting an input/output instruction issued by said CPU to said input/output control apparatuses which has been assigned in advance, and receiving a response from said input/output control apparatus;

a diagnostic control circuit connected with said CPU and said at least one memory and with said input/output control apparatus; and

a single board on which said CPU, said memory, said diagnostic control circuit and said communication means are mounted,

wherein when said diagnostic control circuit detects a fault in said connected CPU and memory installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between a second non-faulty CPU and memory installed apparatus and an input/output control apparatus originally connected to a faulty CPU and memory installed apparatus.

15. (Previously Presented) A CPU and memory installed apparatuses according to claim 14, wherein said communication means comprises:

means for receiving said response as being effective only when the source of the received response is the input/output control apparatuses which has been assigned in advance.

16. (Previously presented) An input/output control apparatus comprising:

an input/output control circuit for controlling a peripheral device based on an input/output instruction; and

communication means for communicating with an external circuit comprising a central processing unit (CPU) and memory installed apparatus and at least one diagnostic control circuit, for receiving an input/output instruction from said CPU and memory installed apparatus which has been set in advance and transferring said input/output instruction to said input/output control circuit, and for transmitting a response to said input/output instruction to

said CPU and memory installed apparatus,

wherein when said diagnostic control circuit detects a fault in said connected CPU and memory installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between a second non-faulty CPU and memory installed apparatus and an input/output control apparatus originally connected to a faulty CPU and memory installed apparatus.

17. (Previously Presented) An input/output control apparatus according to claim 16, wherein said communication means comprises:

means for receiving said input/output instruction as being effective only when the source of the received input/output instruction is the CPU and memory installed apparatus which has been set in advance.

18. (Previously Presented) A computer system according to claim 2, wherein each of said plurality of input/output control apparatuses further comprises an input/output (I/O) device.

19. (Previously Presented) A computer system according to claim 18, wherein said input/output (I/O) device is connected to a peripheral device.

20. (Previously Presented) A computer system according to claim 18, wherein said input/output (I/O) device is connected to a second network.

21. (Withdrawn) The clustered computer system according to claim 1, wherein when one of said plurality of CPU and memory installed apparatuses stops its operation with one of said plurality of input/output control apparatuses, an other one of said plurality of CPU and memory installed apparatuses begins operation with said one of said plurality of input/output control apparatuses.

22. (Previously Presented) The computer system according to claim 2, wherein said communication means comprises a plurality of ports.

23. (Previously Presented) The computer system according to claim 22, wherein each of said plurality of input/output control apparatuses is allocated to at least one of said plurality of ports of said communication means.

24. (Previously Presented) The computer system according to claim 22, wherein when one of the plurality of CPU and memory installed apparatuses stops its operation with one of said plurality of input/output control apparatuses, said one of said plurality of input/output control apparatuses is newly allocated to any one of the plurality of ports to which said one of said plurality of input/output control apparatuses was not previously allocated.